IN THE CLAIMS

The currently pending claims are as follows:

1. (Original) A computer comprising:

a microprocessor; and

a dynamic random access memory (DRAM), coupled to the microprocessor, which includes:

a clock controller;

an address decoder operatively coupled to the clock controller;

an I/O circuit operatively coupled to the clock controller and address decoder; and

a memory array, operatively coupled to the I/O circuit and the address decoder, comprising:

digit line pair;

an internal row address signal (RAS) generator operable to produce an internal RAS in response to an initial power on condition;

a sense amplifier that upon an occurrence of the internal RAS pulse during the initial power on condition drives the digit line pair to opposite rails; and

an equilibration circuit that upon the occurrence of the internal RAS pulse during the initial power on condition equilibrates voltages on the digit line pair to Vcc/2 and permits a common capacitor plate to charge to Vcc/2.

2. (Original) The computer of claim 1, further comprising a voltage generator operatively coupled to the digit line pair.

3. (Original) The computer of claim 2, wherein the sense amplifier and the equilibration circuit have a higher current carrying capacity than the voltage generator.

4. (Original) A computer comprising:

a microprocessor; and

a dynamic random access memory (DRAM), coupled to the microprocessor, which includes:

a clock controller;

an address decoder operatively coupled to the clock controller;

an I/O circuit operatively coupled to the clock controller and address decoder; and

a memory array, operatively coupled to the I/O circuit and the address decoder, comprising:

a voltage generator for providing a stable Vcc/2;

a digit line pair;

a sense amplifier that upon an occurrence on an internally generated RAS pulse during initialization of the DRAM drives the digit line pair to opposite rails; and

an equilibration circuit that upon the occurrence of the internal RAS pulse during the initial power on condition equilibrates voltages on the digit line pair to Vcc/2 to assist the voltage generator in charging a common capacitor plate to Vcc/2 so that the DRAM is enabled for normal operation.

5. (Original) The computer of claim 4, wherein the sense amplifier and the equilibration circuit have a higher current carrying capacity than the voltage generator.

6. (Original) A computer comprising:

a microprocessor; and

a dynamic random access memory (DRAM), coupled to the microprocessor, which includes:

a clock controller;

an address decoder operatively coupled to the clock controller;

an I/O circuit operatively coupled to the clock controller and address decoder; and

a memory array, operatively coupled to the I/O circuit and the address decoder, the memory array comprising:

a digit line pair;

an internal row address signal (RAS) generator operable to produce an internal RAS pulse in response to an initial power on condition;

a sense amplifier constructed and arranged for driving the digit line pair to opposite rails upon an occurrence of the internal RAS pulse during the initial power on condition; and

an equilibration circuit that upon the occurrence of the internal RAS pulse during the initial power on condition equilibrates voltages on the digit line pair to a first equilibrated voltage and permits a common capacitor plate to charge to the first equilibrated voltage.

7. (Original) The computer of claim 6, further comprising a voltage generator operatively coupled to the digit line pair.

8. (Original) The computer of claim 7, wherein the sense amplifier and the equilibration circuit have a higher current carrying capacity than the voltage generator.

9. (Original) A computer comprising:

a microprocessor; and

a dynamic random access memory (DRAM), coupled to the microprocessor, which includes:

a clock controller;

an address decoder operatively coupled to the clock controller;

an I/O circuit operatively coupled to the clock controller and address decoder; and

a memory array, operatively coupled to the I/O circuit and the address decoder, comprising:

a digit line pair;

an internal row address signal (RAS) generator operable to produce an internal RAS pulse in response to an initial power on condition, wherein the initial power on condition occurs during power up of the DRAM and prior to memory cell access;

a sense amplifier that upon an occurrence of the internal RAS pulse during the initial power on condition drives the digit line pair to opposite rails; and

an equilibration circuit that upon the occurrence of the internal RAS pulse during the initial power on condition equilibrates voltages on the digit line pair to Vcc/2 and permits a common capacitor plate to charge to Vcc/2.

10. (Original) The computer of claim 9, further comprising a voltage generator operatively coupled to the digit line pair.

11. (Original) The computer of claim 10, wherein the sense amplifier and the equilibration circuit have a higher current carrying capacity than the voltage generator.

12. (Original) A computer comprising:

a microprocessor; and

a dynamic random access memory (DRAM), coupled to the microprocessor, which includes:

a clock controller;

an address decoder operatively coupled to the clock controller;

an I/O circuit operatively coupled to the clock controller and address decoder; and

a memory array, operatively coupled to the I/O circuit and the address decoder, comprising:

a voltage generator for providing a stable Vcc/2;

a digit line pair;

a sense amplifier that drives the digit line pair to opposite rails upon an occurrence on an internally generated RAS pulse produced in response to an initial power on condition, wherein the initial power on condition occurs during power up of the DRAM and prior to memory cell access; and

an equilibration circuit that upon the occurrence of the internal RAS pulse during the initial power on condition equilibrates voltages on the digit line pair to Vcc/2 to assist the voltage generator in charging a common capacitor plate to Vcc/2 so that the DRAM is enabled for normal operation.

13. (Original) The computer of claim 12, wherein the sense amplifier and the equilibration circuit have a higher current carrying capacity than the voltage generator.

14. (Original) A computer comprising:

a microprocessor; and

a dynamic random access memory (DRAM), coupled to the microprocessor, which includes:

a clock controller;

an address decoder operatively coupled to the clock controller;

an I/O circuit operatively coupled to the clock controller and address decoder; and

a memory array, operatively coupled to the I/O circuit and the address decoder, the memory array comprising:

a digit line pair;

an internal row address signal (RAS) generator operable to produce an internal RAS pulse in response to an initial power on condition, wherein the initial power on condition occurs during power up of the DRAM and prior to memory cell access;

a sense amplifier constructed and arranged for driving the digit line pair to opposite rails upon an occurrence of the internal RAS pulse during the initial power on condition; and

an equilibration circuit that upon the occurrence of the internal RAS pulse during the initial power on condition equilibrates voltages on the digit line pair to a first equilibrated voltage and permits a common capacitor plate to charge to the first equilibrated voltage.

15. (Original) The computer of claim 14, further comprising a voltage generator operatively coupled to the digit line pair.

16. (Original) The computer of claim 15, wherein the sense amplifier and the equilibration circuit have a higher current carrying capacity than the voltage generator.

17. (Original) A computer comprising:

a microprocessor; and

a dynamic random access memory (DRAM), coupled to the microprocessor, which includes:

a clock controller;

an address decoder operatively coupled to the clock controller;

an I/O circuit operatively coupled to the clock controller and address decoder; and

a memory array, operatively coupled to the I/O circuit and the address decoder, comprising:

a digit line pair;

a signal generator operable to produce a pulse in response to an initial power on condition, wherein the initial power on condition occurs during power up of the DRAM and prior to memory cell access;

a sense amplifier that upon an occurrence of the pulse during the initial power on condition drives the digit line pair to opposite rails; and

an equilibration circuit that upon the occurrence of the pulse during the initial power on condition equilibrates voltages on the digit line pair to Vcc/2 and permits a common capacitor plate to charge to Vcc/2.

18. (Original) The computer of claim 17, further comprising a voltage generator operatively coupled to the digit line pair.

19. (Original) The computer of claim 18, wherein the sense amplifier and the equilibration circuit have a higher current carrying capacity than the voltage generator.

20. (Original) The computer of claim 17, wherein the signal generator includes an internal row address signal (RAS) generator operable to produce the pulse as an internal RAS pulse in response to the initial power on condition.

21. (Original) A computer comprising:

a microprocessor; and

a dynamic random access memory (DRAM), coupled to the microprocessor, which includes:

a clock controller;

an address decoder operatively coupled to the clock controller;

an I/O circuit operatively coupled to the clock controller and address decoder; and

a memory array, operatively coupled to the I/O circuit and the address decoder, the memory array having multiple memory segments, and the memory array further comprising:

at least one digit line pair;

a signal generator operable to produce multiple pulses in response to an initial power on condition, wherein the initial power on condition occurs during power up of the DRAM and prior to memory cell access;

a sense amplifier, operable to drive a digit line pair of one or more memory segments to opposite rails in response to a first pulse received from the signal generator, and operable to drive digit line pairs of other memory segments in response to additional pulses received from the signal generator; and

an equilibration circuit, operable to equilibrate voltages on the digit line pair of the one or more memory segments to Vcc/2 and to permit a common capacitor plate to charge to Vcc/2, in response to the first pulse, and to equilibrate voltages on the digit line pairs of the other memory segments in response to the additional pulses.

22. (Original) The computer of claim 21, further comprising a voltage generator operatively coupled to the at least one digit line pair.

23. (Original) The computer of claim 22, wherein the sense amplifier and the equilibration circuit have a higher current carrying capacity than the voltage generator.

24. (Original) The computer of claim 21, wherein the signal generator includes an internal row address signal (RAS) generator operable to produce the first pulse as an internal RAS pulse in response to the initial power on condition.